Hardware Accelerated Collision Detection

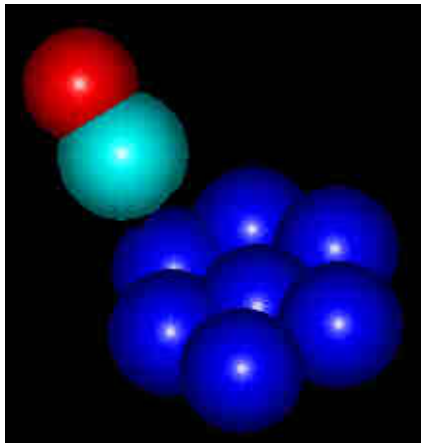
– An Architecture and Simulation Results

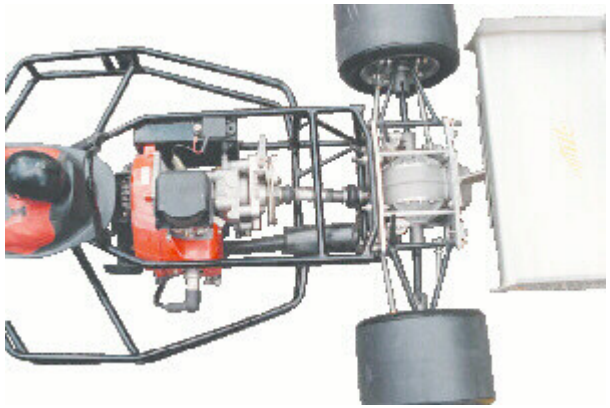
by Andreas Raabe,[1] Blazej Bartyzel,[1]
Gabriel Zachmann,[2] Joachim K. Anlauf [1]

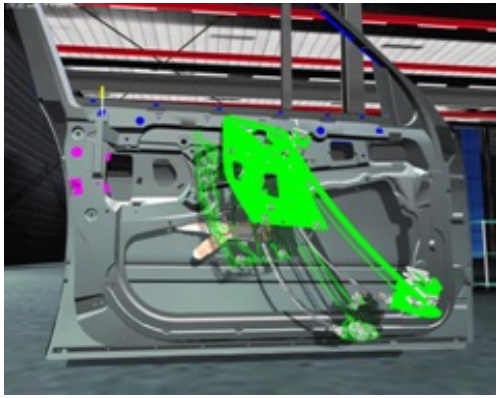
Institut für Informatik
[2]Computer-Graphik [1]Technische Informatik
universitätbonn

What is Collision Detection?

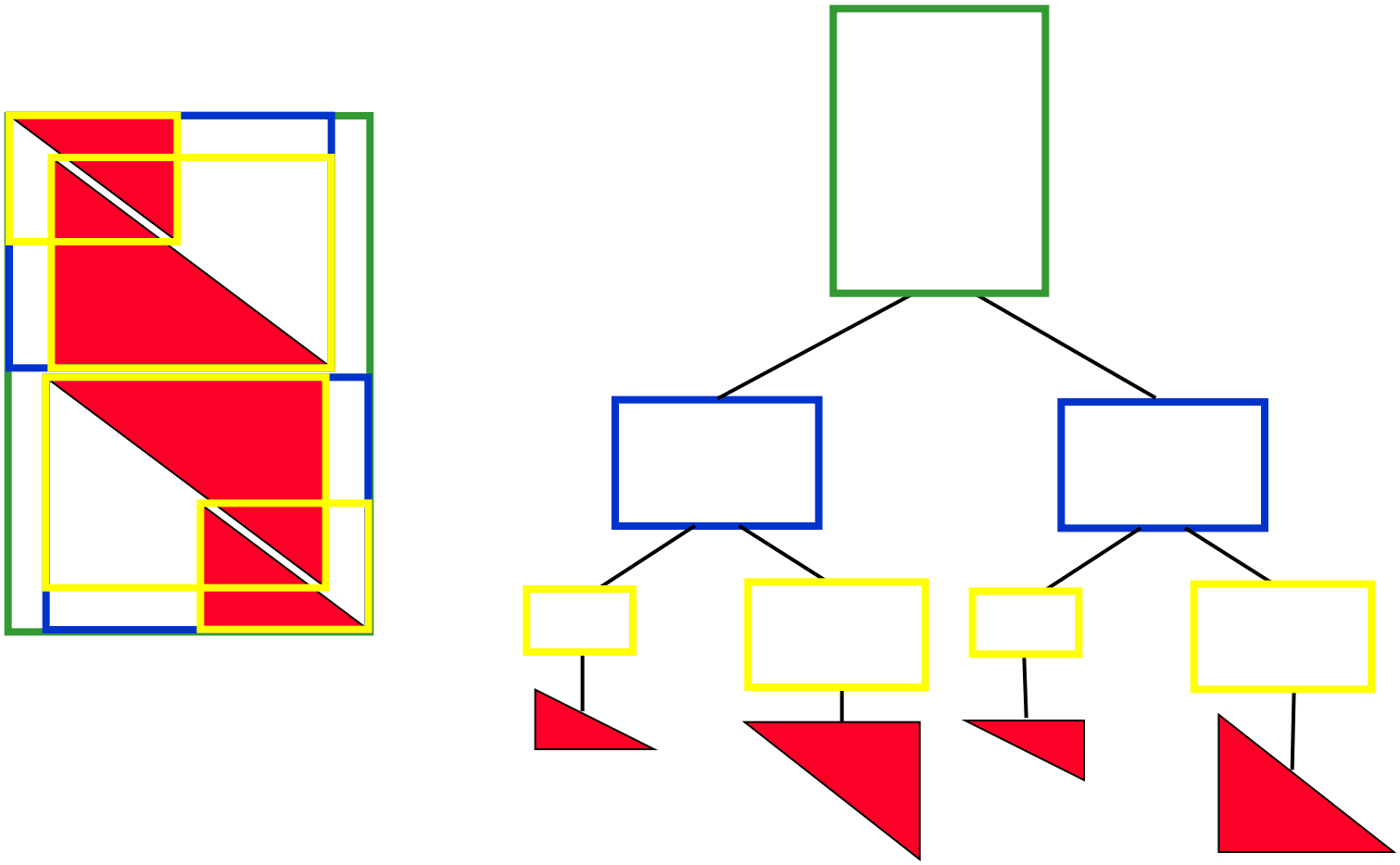
Applications





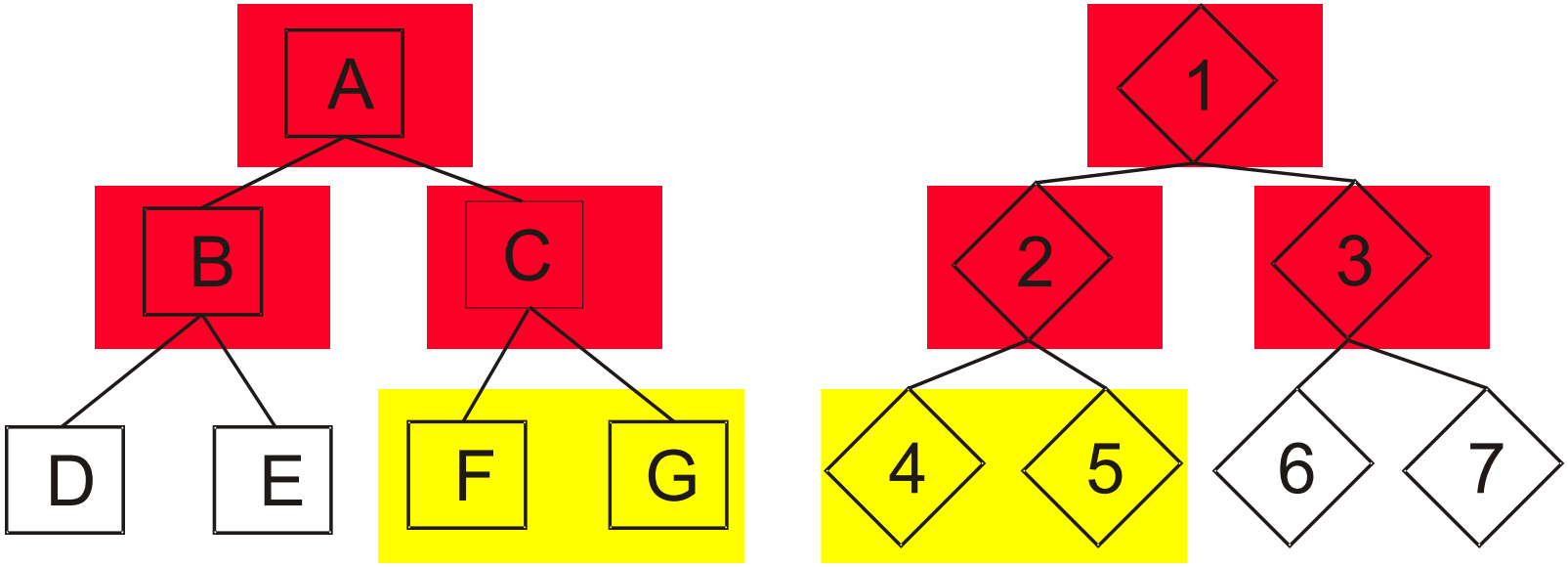


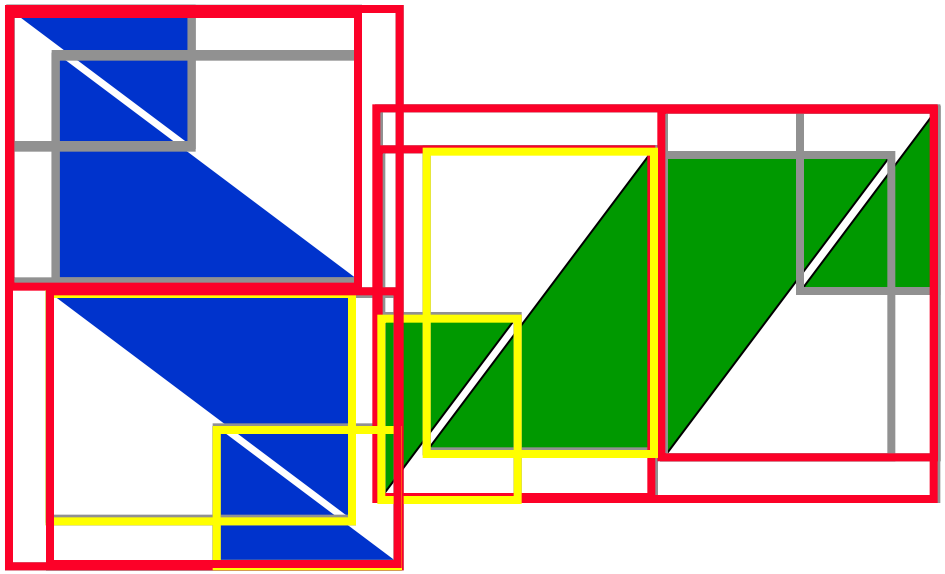
Bounding-Volume Hierarchy



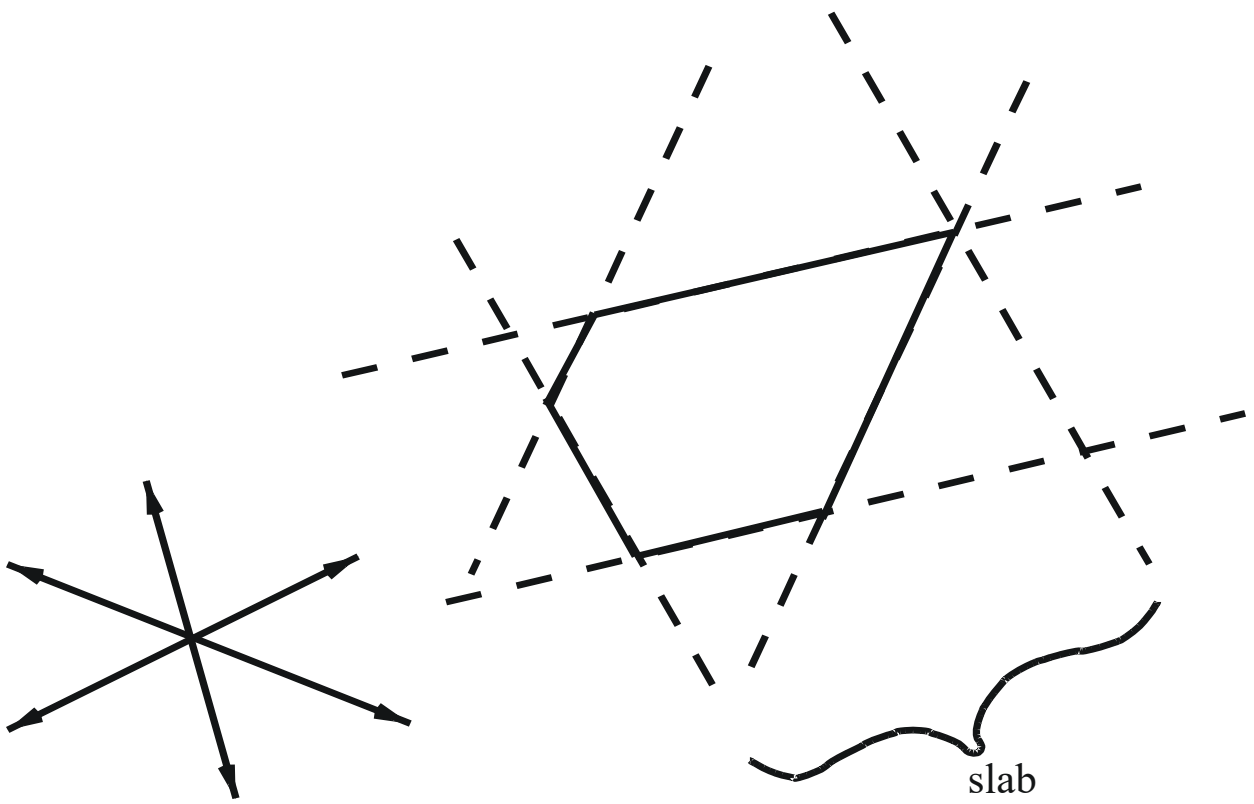
Bounding Volumes enclose ALL volumes on lower levels of the hierarchy and can be checked for collision fastly.

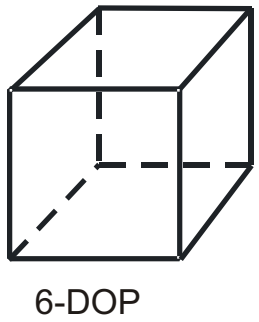
Hierarchical Collision Detection



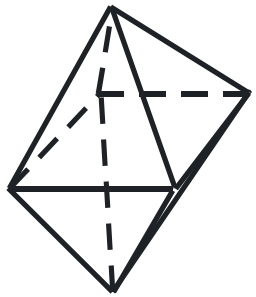


k-DOPs

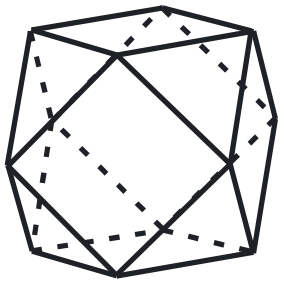




6-DOP



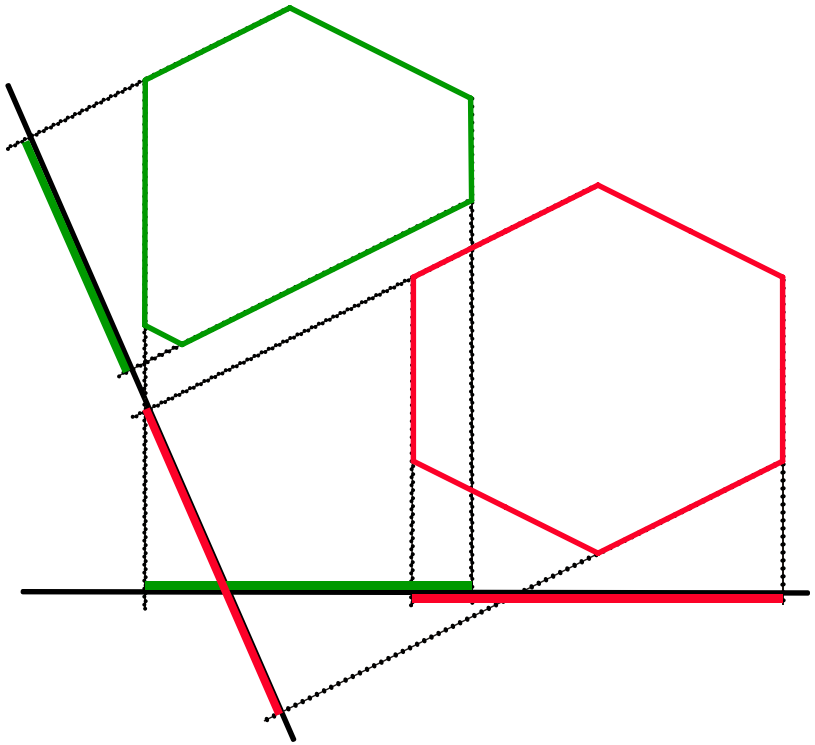
8-DOP



14-DOP

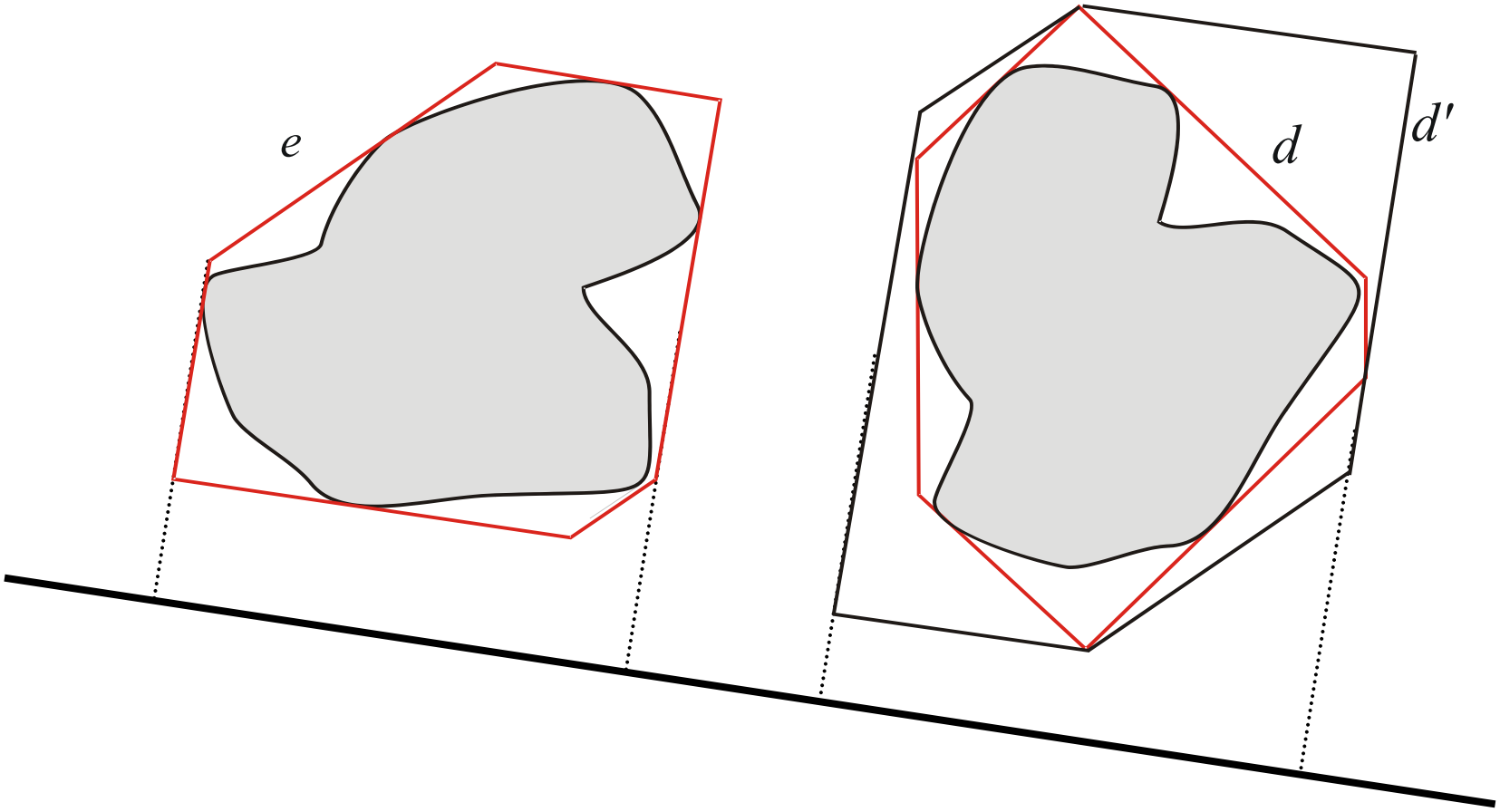
A DOP consists of *k/2* pairs of antiparallel hyperplanes with fixed orientation.

Check For Overlap



If one slab-pair does not overlap the DOPs are not intersecting.

Enclosing DOP



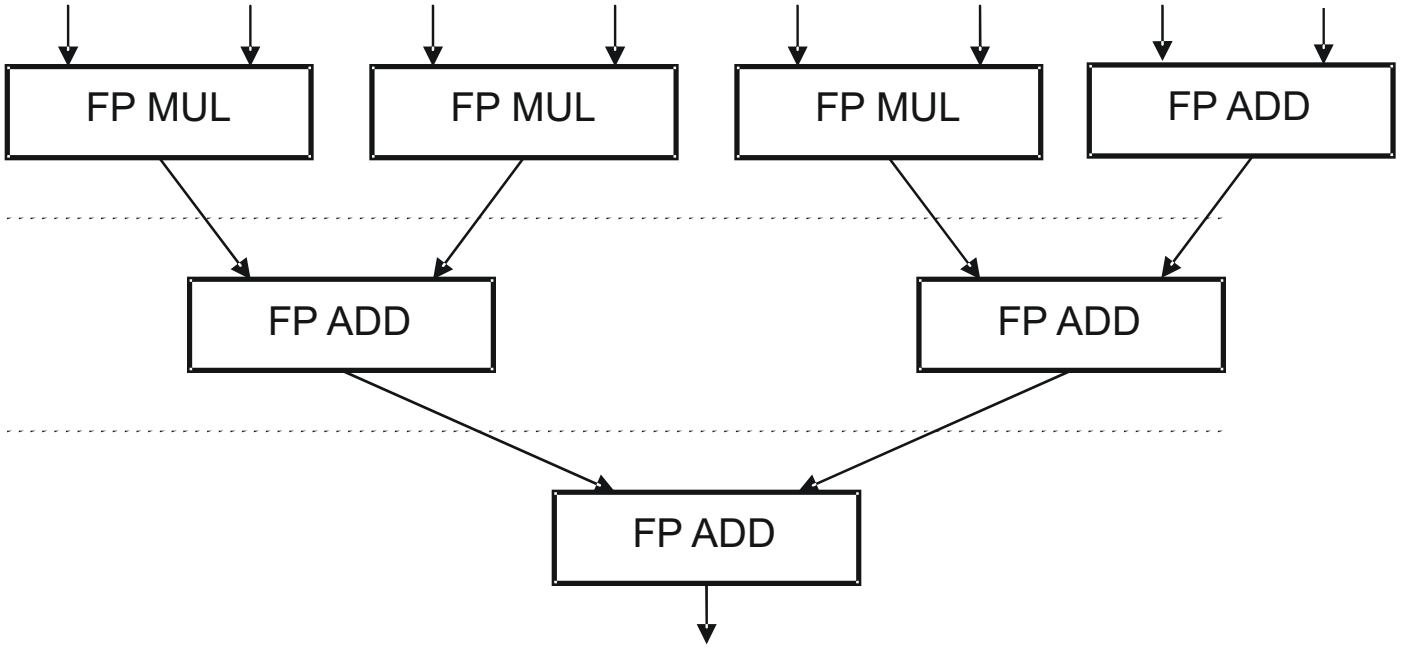
To check for intersection DOP *d* is enclosed with another DOP *d´* with the same orientations as *e*.

Rotation and translation

$$\begin{pmatrix} d'_0 \\ d'_1 \\ d'_2 \\ \dots \\ d'_{k-3} \\ d'_{k-2} \\ d'_{k-1} \end{pmatrix} = \begin{pmatrix} 0 & 0 & C_{1_0} & 0\dots0 & 0 & C_{1_1} & C_{1_2} \\ C_{2_0} & 0 & C_{2_1} & 0\dots0 & C_{2_2} & 0 & 0 \\ 0 & C_{2_0} & 0 & 0\dots0 & C_{2_1} & C_{2_3} & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ C_{2_0} & C_{2_1} & 0 & 0\dots0 & 0 & C_{2_2} & 0 \\ 0 & C_{2_0} & C_{2_1} & 0\dots0 & C_{2_2} & 0 & 0 \\ 0 & 0 & C_{2_0} & C_{2_1} & 0 & C_{2_2} & 0 \end{pmatrix} * \begin{pmatrix} d_0 \\ d_1 \\ d_2 \\ \dots \\ d_{k-3} \\ d_{k-2} \\ d_{k-1} \end{pmatrix} + \begin{pmatrix} c_0 \\ c_1 \\ c_2 \\ \dots \\ c_{k-3} \\ c_{k-2} \\ c_{k-1} \end{pmatrix}$$

DOP Transformation Unit

$$\tilde{d}'_i = d_k C_{i_0} + d_m C_{i_1} + d_n C_{i_2} + c_i + e_{i+k/2}$$



=> further refinement into 15 pipeline stages

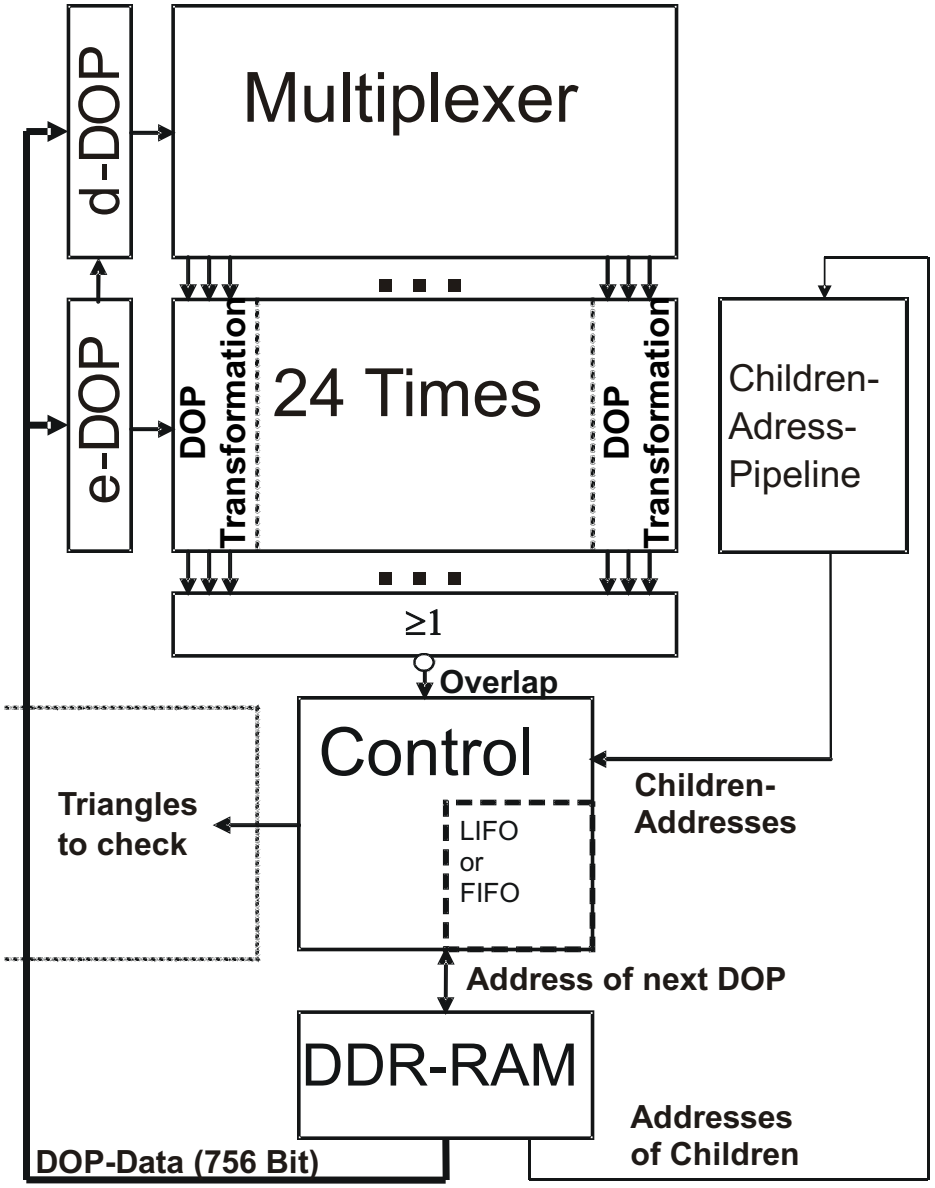
The DOP Testing Unit

A multiplexer routes the d's to the corresponding transformation unit in the criterion checker.

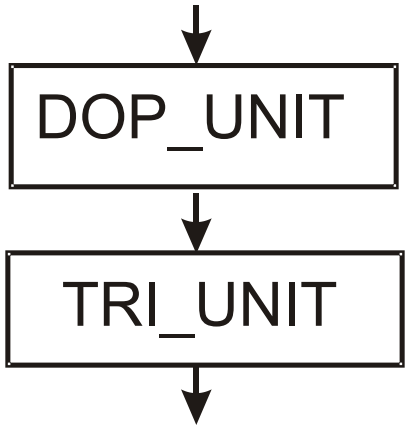
24 transformations and slap-overlap tests

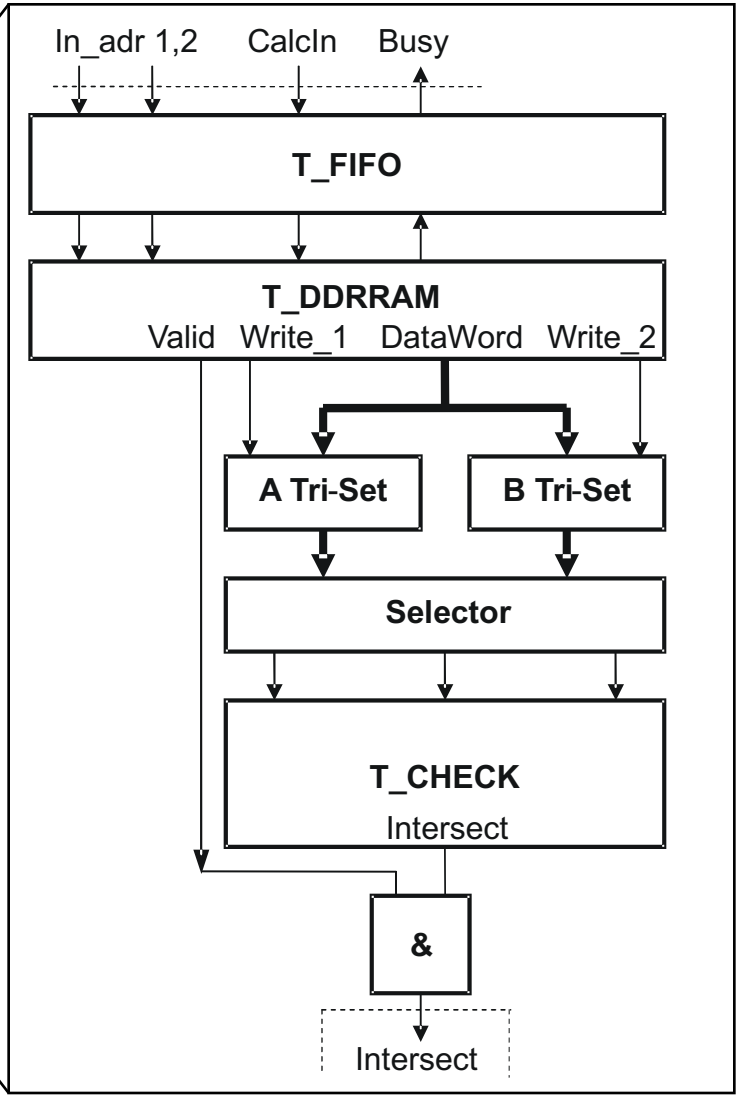
NOR

If the DOPs intersect the next level of the hierarchy is fetched from memory. If a leaf is reached the according triangles are checked for intersection.



Triangle Intersection





The Triangle Intersection Test (T_CHECK) consists of 52 pipeline stages.

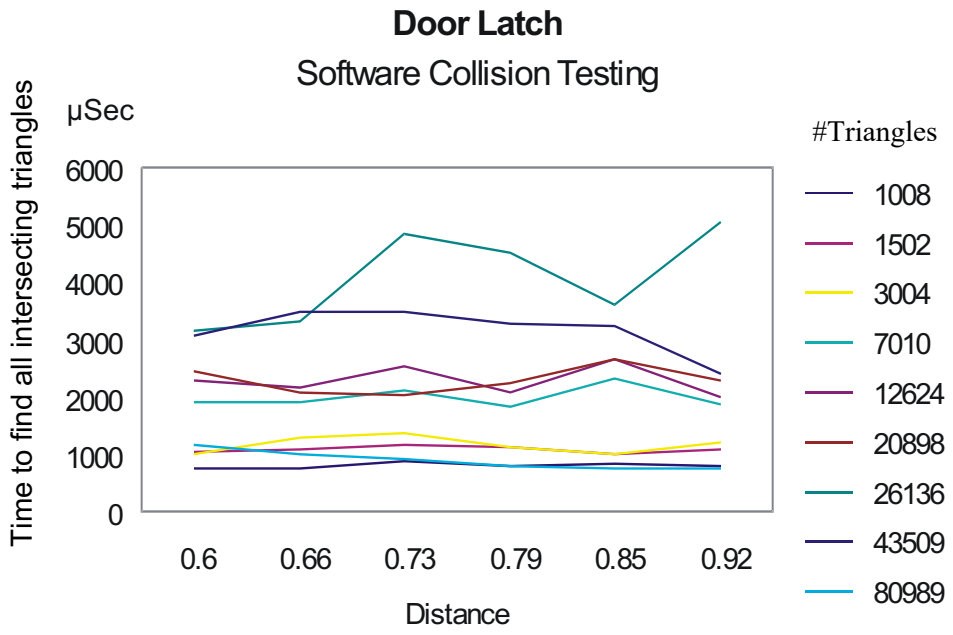
Benchmark

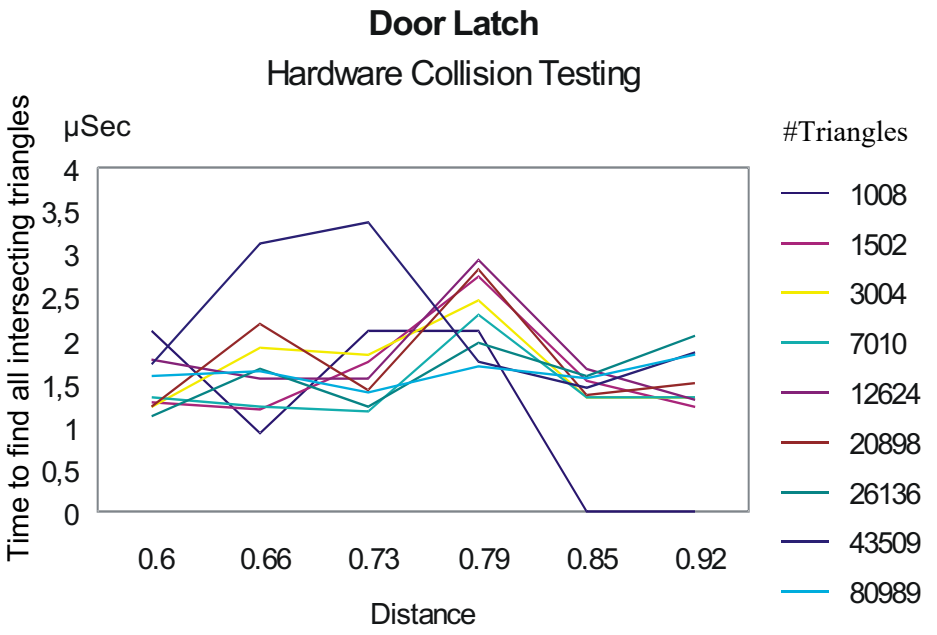
- Converge two identical objects
- Rotate one
- Average time for every distance to find all intersecting triangles

Benchmarking Results

Software version running on a 1GHz Pentium 3

VHDL-Simulation targeting a NEC CMOS ASIC (CB-130 UX5, 800 MHz) running at 266MHz





Speed-Up of serveral orders of magnitude

universitätbonn

Future Work

- Implementation on an FPGA
- Comparison of different Bounding-Volumes
- Compression of Bounding-Volume Hierarchy in Memory
- Hardware collision-testing of different primitives
- Further investigation in different traversal strategies

Summary

- **Design of**
  - **a DOP intersection test hardware**
  - **a triangle intersection test hardware**
  - **a control-unit**
- **Simulation in VHDL**
- **Benchmarks**
  - **of complete design**
  - **of different traversal strategies**

DFG-Project ZA292/2-1